WHAT IS CLAIMED IS:

1. A method for fabricating a metal-insulator-metal capacitor, comprising:

forming a first metal layer;

forming a first insulating layer on the first metal layer;

forming at least a first opening and at least a second opening in the first insultaing layer;

depositing a mask over the second opening;

forming a first dielectric layer in the first opening;

removing the mask;

depositing a first conductive material in the first and second openings; and

depositing a second metal layer over the first and second openings.

2. The method as recited in claim 1, further comprising forming a polish stop layer on the first insulating layer.

3. The method as recited in claim 1, wherein the first and second openings are formed by etching the insulating layer down to the first metal layer.

4. The method as recited in claim 1, further comprising performing chemical mechanical polishing on the conductive material.

5. The method as recited in claim 1, wherein the second metal layer consists of a first plate formed over the first opening and a second plate formed over the second opening.

6. The method as recited in claim 1, further comprising:

forming a second insulating layer on the second metal layer;

forming at least a third opening and at least a fourth opening in the second insultaing layer;

forming a second dielectric layer in the third opening;

depositing a second conductive material in the third and fourth openings; and

forming a third metal layer over the third and fourth openings.

7. The method as recited in claim 1, wherein the first and second metal layers are formed from one of aluminum, copper and tungsten.

8. The method as recited in claim 1, wherein the mask is formed from one of a polymer or resist material.

9. The method as recited in claim 1, wherein the first conductive material is formed from one of aluminum, copper and tungsten.

10. The method as recited in claim 1, wherein the first dielectric layer is formed from one of chemical vapor deposition oxide and chemical vapor deposition nitride.

11. A method for fabricating a metal-insulator-metal capacitor, comprising:

forming a first metal layer;

forming an insulating layer on the first metal layer;

forming at least a first via and at least a second via in the insulting layer and on the first metal layer;

depositing a mask over the second via and a predetermined portion of the insulating layer;

etching an exposed area of the insulating layer down to the first metal layer;

removing the mask;

forming a dielectric layer on a remaining area after etching and removal of the mask;

selectively removing a predetermined portion of the dielectric layer; and

depositing a second metal layer over the first and second vias.

12. The method as recited in claim 11, wherein the first and second vias include conductive material deposited therein.

13. The method as recited in claim 11, further comprising forming a polish stop layer on the insulating layer.

14. The method as recited in claim 11, wherein the predetermined portion of the dielectric layer covers at least the second via.

15. The method as recited in claim 11, further comprising patterning the second metal layer to form a first plate over the first via and a second plate over the second via.

16. The method as recited in claim 11, wherein the first and second metal layers are formed from one of aluminum, copper and tungsten.

17. The method as recited in claim 11, wherein the mask is formed from one of a polymer or resist material.

18. The method as recited in claim 11, wherein the dielectric layer is formed from one of chemical vapor deposition oxide and chemical vapor deposition nitride.

19. A method for fabricating a metal-insulator-metal capacitor, comprising:

forming a first metal layer;

forming an insulating layer on the first metal layer;

forming at least a first opening and at least a second opening in the insultaing layer;

depositing a sidewall liner material on the insulating layer and in the first and second openings;

removing a predetermined portion of the sidewall liner material to form spacers on each sidewall of the first and second openings;

forming a dielectric layer on the insulating layer, and on the spacers and exposed portions of the first metal layer in the first and second openings;

depositing a mask over at least the first opening;

removing the dielectric layer from at least the second opening;

filling the second opening with a conductive material; and

depositing a second metal layer over and in the first opening and over the second opening including the conductive material.

20. The method as recited in claim 19, wherein the first and second openings are formed by etching the insulating layer down to the first metal layer.

21. The method as recited in claim 19, wherein the sidewall liner material is TiN.

22. The method as recited in claim 19, wherein the step of removing a predetermined portion of the sidewall liner material is performed by etching the sidewall liner material.

23. The method as recited in claim 19, wherein the mask is formed from one of a polymer or resist material.

24. The method as recited in claim 19, wherein the step of removing the dielectric layer is performed by selective etching.

25. The method as recited in claim 19, wherein the conductive material is formed from one of aluminum, copper and tungsten.

26. The method as recited in claim 19, further comprising patterning the second metal layer to form a first plate over and in the first opening and a second plate over the second opening including the conductive material.

27. The method as recited in claim 19, wherein the first and second metal layers are formed from one of aluminum, copper and tungsten.

28. The method as recited in claim 19, wherein the dielectric layer is formed from one of chemical vapor deposition oxide and chemical vapor deposition nitride.

29. A metal-insulator-metal capacitor, comprising:

a metal layer;

an insulating layer formed on the metal layer;

at least a first opening and at least a second opening formed in the first insultaing layer;

a dielectric layer formed in the first opening;

a conductive material deposited in the first and second openings; and

a first metal plate formed over the first opening and a second metal plate formed over the second opening.

30. The metal-insulator-metal capacitor as recited in claim 29, further comprising a polish stop layer formed on the insulating layer.

31. The metal-insulator-metal capacitor as recited in claim 29, wherein the metal layer and the first and second metal plates are formed from one of aluminum, copper and tungsten.

32. The metal-insulator-metal capacitor as recited in claim 29, wherein the conductive material is formed from one of aluminum, copper and tungsten.

33. The metal-insulator-metal capacitor as recited in claim 29, wherein the dielectric layer is formed from one of chemical vapor deposition oxide and chemical vapor deposition nitride.

34. A metal-insulator-metal capacitor, comprising:

a metal layer;

an insulating layer formed on the metal layer;

at least a first via and at least a second via formed in the insulting layer and on the metal layer;

a dielectric layer formed on the first via and on an exposed area of the metal layer; and

a first metal plate formed over the first via and a second metal plate formed over the second via.

35. The metal-insulator-metal capacitor as recited in claim 34, wherein the first and second vias include conductive material deposited therein.

36. The metal-insulator-metal capacitor as recited in claim 34, further comprising a polish stop layer formed on the insulating layer.

37. The metal-insulator-metal capacitor as recited in claim 34, wherein the metal layer and the first and second metal plates are formed from one of aluminum, copper and tungsten.

38. The metal-insulator-metal capacitor as recited in claim 34, wherein the dielectric layer is formed from one of chemical vapor deposition oxide and chemical vapor deposition nitride.

39. A metal-insulator-metal capacitor, comprising:

a metal layer;

an insulating layer formed on the metal layer;

at least a first opening and at least a second opening formed in the insultaing layer;

spacers formed on each sidewall of the first and second openings;

a dielectric layer lining the spacers and bottom wall of the first opening;

a conductive material deposited in the second opening; and

a first metal plate formed over and in the first opening and a second metal plate formed over the second opening including the conductive material.

40. The metal-insulator-metal capacitor as recited in claim 39, wherein the spacers are formed of TiN.

41. The metal-insulator-metal capacitor as recited in claim 39, wherein the conductive material is formed from one of aluminum, cooper and tungsten.

42. The metal-insulator-metal capacitor as recited in claim 39, wherein the metal layer and the first and second metal plates are formed from one of aluminum, copper and tungsten.

43. The metal-insulator-metal capacitor as recited in claim 39, wherein the dielectric layer is formed from one of chemical vapor deposition oxide and chemical vapor deposition nitride.

44. A method for fabricating a metal-insulator-metal capacitor, comprising:

forming at least a first via for incorporation into the metal-insulator-metal capacitor; and

forming, simultaneously with formation of the first via, at least a second via for incorporation into a BEOL interconnect.

45. A method for fabricating a semiconductor device, comprising:

forming at least one metal-insulator-metal capacitor; and

forming, simultaneously with formation of the at least one metal-insulator-metal capacitor, at least one BEOL interconnect.